Exercise of Electronics for Communication Systems Prof. C. Abbate, G. Busatto - A.A. 2018/2019

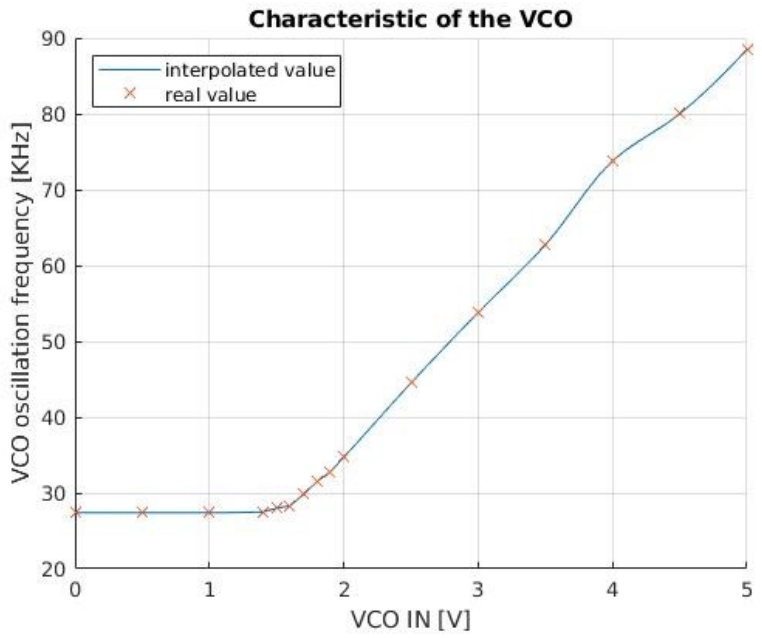
10 – Experimental characterization of the integrated PLL (HCF4046B)

29/11/2018 – Diego Tuzi – 50435 – diego.tuzi@studentmail.unicas.it

TEST OF VCO OPERATION

Place the components R1, R2 and C1 on the board. The supply voltage is 5 V. Connect the voltage supplied by the second section of the power supply to the pin 9 (VCO IN). In alternative use a second power supply. Measure the characteristic of the VCO. For this purpose measure the oscillation frequency of the VCO for VCO IN variable between 0 and 5V with 0.5V steps.

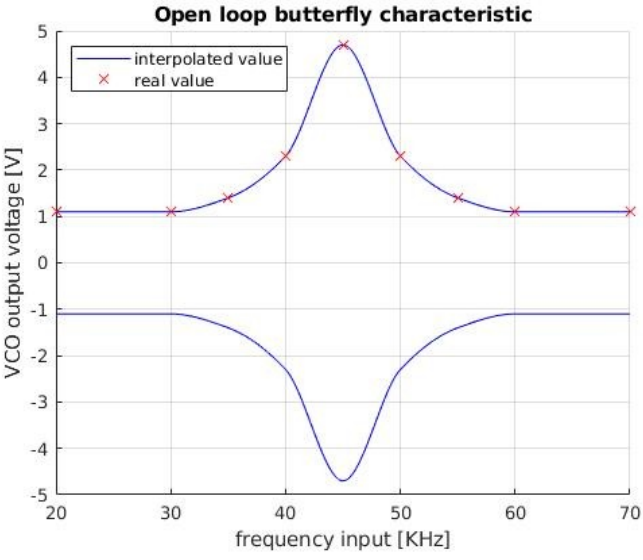
VCO [V]	VCO oscillation freq. [KHz]
0.00	27.40
0.50	27.40
1.00	27.40
1.40	27.50
1.50	28.00
1.60	28.30
1.70	29.80
1.80	31.50
1.90	32.80
2.00	34.70
2.50	44.50
3.00	53.80
3.50	62.70
4.00	73.80
4.50	80.00
5.00	88.50



OPEN LOOP BUTTERFLY CHARACTERISTIC

Remove R3 e C2 and connect the supplied external RC circuit in order to leave open the feed-back loop.
Supply pin 9 (VCO IN) with a voltage of 2.5 V given by the second section of the power supply. Supply pin 14 (BNC connector IN) with a square waveform given by a signal generator with the amplitude of 4.5 V and duty-cycle 50%. Measure the characteristic Vc= g(fi) (the voltage across C2), where fi is the frequency of the input signal.
Do it for phase comparators I. For measuring the characteristic connect the oscilloscope probes to “BNC connector IN” and capacitor C2.

Fi [KHz]	Vc= g(fi) [V]
20.00	1.10
30.00	1.10
35.00	1.40
40.00	2.30
45.00	4.70
50.00	2.30
55.00	1.40



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Do it for phase comparators II. For measuring the characteristic connect the oscilloscope probes to “BNC connector IN” and capacitor C2.

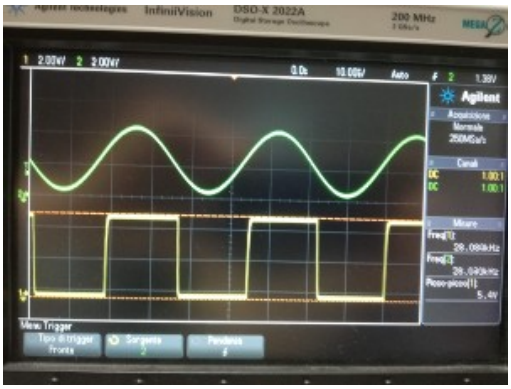
Using phase comparator II, circuit is unstable.

CLOSED LOOP BUTTERFLY CHARACTERISTIC

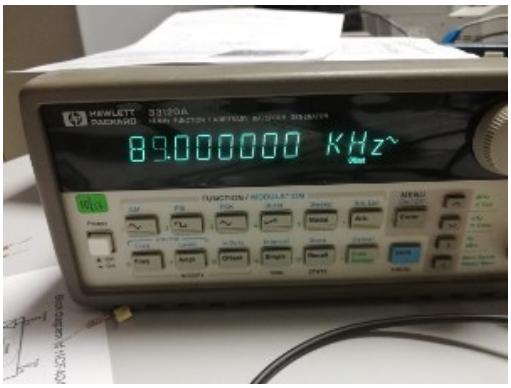
Close the feedback loop disconnecting the external RC and then connecting the components R3, C2 in the specific sockets.
Select phase comparator II (Jumper SELECT COMP on COMP2).
Supply pin 14 (BNC connector IN) with a square waveform given by a signal generator with amplitude 4.5 V and duty-cycle 50%.
Starting from low input frequencies fi (100Hz) visualize the voltage waveform on pin 10 (DEM OUT) which reproduce the voltage at pin 9 (VCO IN) thanks to a voltage follower present in the integrated circuit. Measure the amplitude of VCO IN varying fi in order to identify the capture and holding frequency for increasing fi.

As you can expect from Design Information Datasheet frequency lock range and frequency hold in range are the same using Phase Comparator II.			
$f_L min$	$f_L max$	$f_H min$	$f_H max$
28 KHz	**89 KHz**	**28 KHz**	**89 KHz**

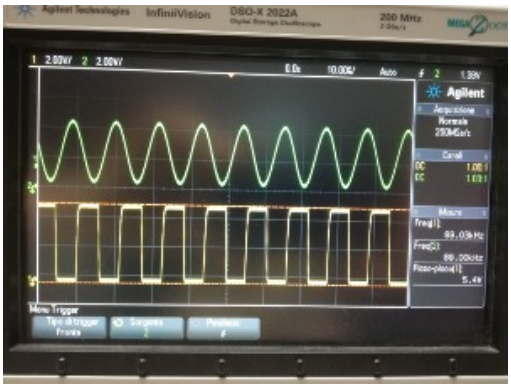
Sine generator
Amplitude=4.5V; Frequency=28KHz



Oscilloscope
IN1 (yellow): voltage waveform on DEM OUT f=28KHz
IN2 (green): Sine generator f=28KHz



Sine generator
Amplitude=4.5V; Frequency=89KHz



Oscilloscope
IN1 (yellow): voltage waveform on DEM OUT f=89KHz
IN2 (green): Sine generator f=89KHz

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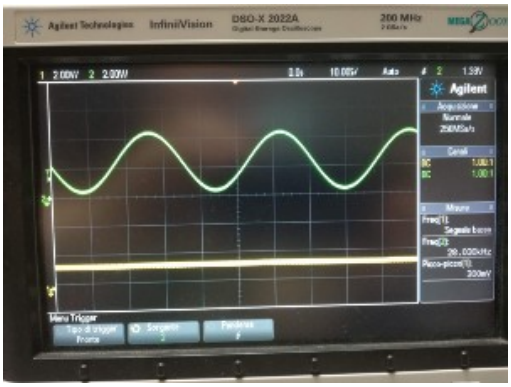
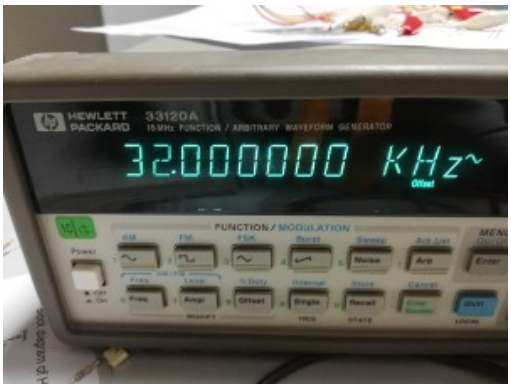
Identify capture and hold ranges of the PLL having selected the phase discriminator I (Jumper SELECT COMP on COMP1).

As you can expect from Design Information Datasheet frequency lock range and frequency hold in range are different using Phase Comparator I. In particular lock range is contained in hold-in range.			
$f_L min$	$f_L max$	$f_H min$	$f_H max$
32 KHz	**58 KHz**	**28 KHz**	**86 KHz**

Sine generator
Amplitude=4.5V; Frequency=28KHz



Oscilloscope
IN1 (yellow): voltage waveform on DEM OUT
IN2 (green): Sine generator f=28KHz
OUT OF CAPTURE RANGE



Sine generator
Amplitude=4.5V; Frequency=32KHz

Oscilloscope
IN1 (yellow): voltage waveform on DEM OUT
IN2 (green): Sine generator f=32KHz
NEW CAPTURE RANGE

Verify the existence of secondary capture ranges for higher values of fi.

PLL locks is able to lock in other frequency range, but the followed frequencies are wrong.			
$f_L min$	$f_L max$	$f_H min$	$f_H max$
121 KHz	**147 KHz**	**92 KHz**	**180 KHz**

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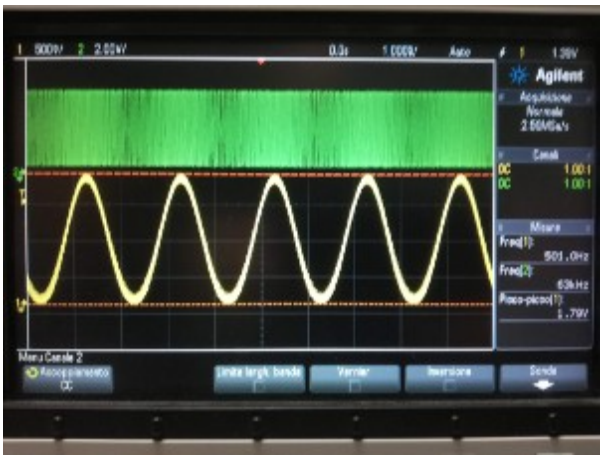
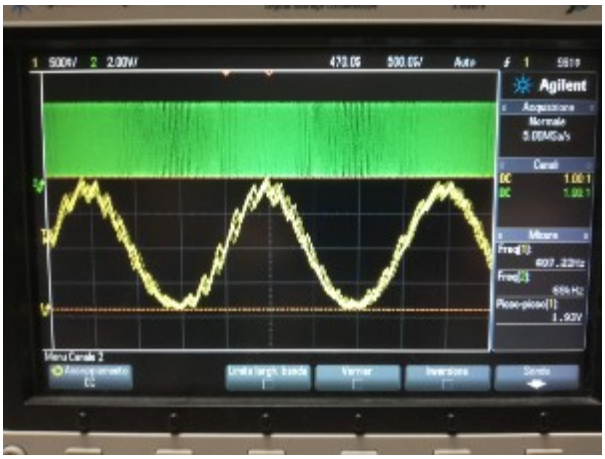
FREQUENCY DEMODULATOR

Feed the input of the PLL with an FM signal with the carrier at 50kHz modulated with a sinusoidal signal at 500Hz, obtained by the HP function generator. Visualize the waveforms on the oscilloscope at the pin DEM OUT.

You can note that PLL can act as FM demodulator.

Using PC I	Using PC II
	
Oscilloscope	**Oscilloscope**
IN1 (yellow): voltage waveform on DEM OUT f=500Hz IN2 (green): FM signal generator fc=50KHz mod=500Hz	IN1 (yellow): voltage waveform on DEM OUT f=500Hz IN2 (green): FM signal generator fc=50KHz mod=500Hz